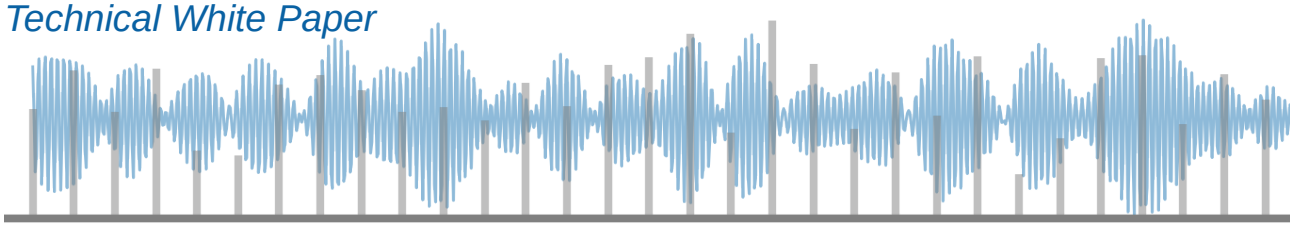


On digital synthesis and detection of microwave signals for quantum technology

Recent progress with integrated circuits for real-time digital signal processing enables a direct digital approach to synchronous drive and measurement of continuous or pulsed microwaves. High-speed data converters give direct access to microwave bands without analog IQ mixers, removing local-oscillator leakage, nonlinear distortion, calibration and drift when controling and measuring quantum circuits. Multiple channels of drive and readout are processed on one chip, replacing racks of expensive equipment and eliminating problems of synchronization and software control of multiple instruments.

RFSoC Technology

5G radio telecommunication has driven the recent development of Radio-Frequency System-on-a-Chip (RFSoC) technology. This acronym designates the chip-level integration of high-speed analog-to-digital converters (ADC), digital-to-analog converters (DAC), a field-programmable gate array (FPGA) and multiple CPU cores. The high density of components and reduced signal-propagation delay enable the interleaving of several slower ADCs to achieve sampling rates up to 5 Gs/s, 10 GS/s for DACs, on 16 parallel channels, all phase coherent and synchronized to one master clock. This extremely high data throughput and processing power creates an ideal platform for a fully programmable, direct digital control and measurement system for microwave quantum technology.

One immediate advantage of RFSoC is the elimination of analog mixers used to up-convert and down-convert signals to microwave frequencies. Analog mixers are nonlinear components with harmonic and intermodulation distortion. They require a separate Local Oscillator (LO) which leaks through, giving unwanted frequency content. Frequency-dependent gain and phase imbalance in the IQ mixer makes it difficult to select a single sideband [1]. This white paper describes direct digital methods which eliminate these problems.

Digital Down- and Up-Conversion

Traditional digital methods limit the maximum frequency in a waveform to the Nyquist frequency, or half the sampling frequency, f_N=½ f_s. To access frequencies above f_N a local oscillator and analog mixer are used to down-convert or up-convert the waveform to another frequency band. Digital methods perform this conversion without mixers by working in a higher Nyquist Zone (NZ) of the ADC or DAC, where frequency content appears at so-called alias frequencies (see fig. 1).

When a high frequency signal is down-converted from a higher Nyquist zone, it is under-sampled by the ADC and it will appear at an alias frequency. Traditional Digital Signal Processing (DSP) removes

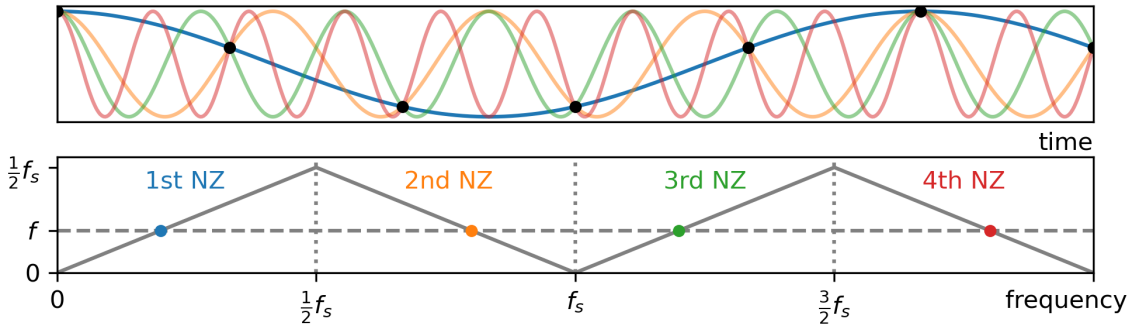


Figure 1: Aliasing and Nyquist Zones: *Discrete periodic samples at frequency f_s represent a sinusoidal signal at frequency f (blue curve). The same set of samples represents under-sampled sinusoids at frequencies in higher Nyquist zones (NZ). Aliasing of a signal at frequency f occurs at frequencies mirrored about integer multiples of the sampling frequency, $nf_s \pm f$ (lower panel).*

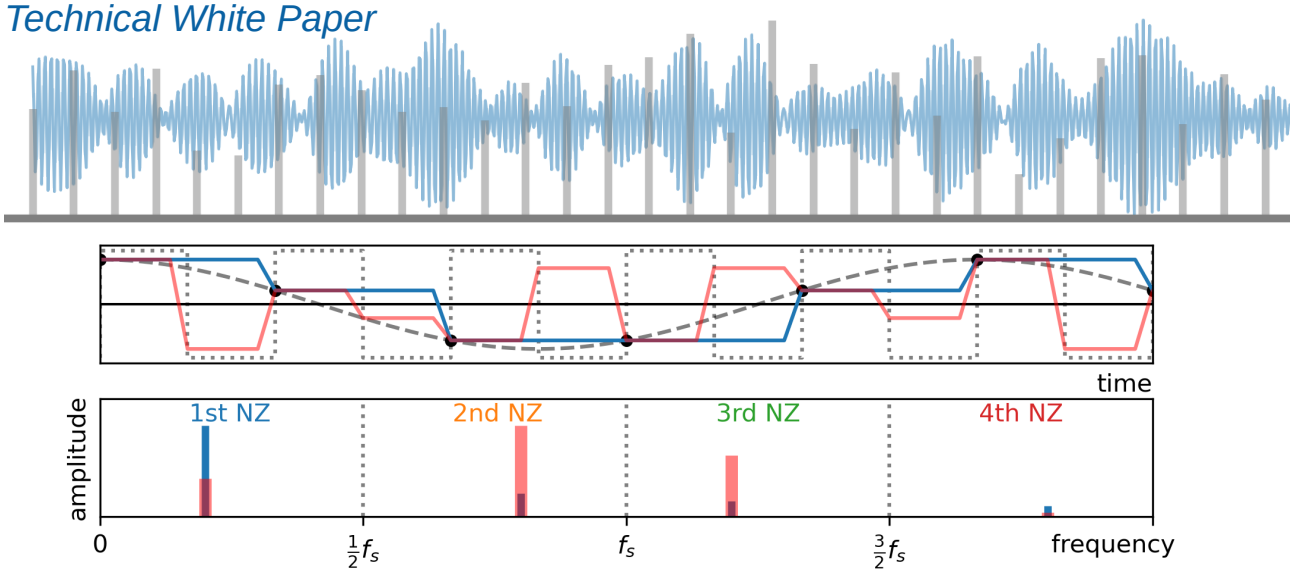


Figure 2: *The DAC performs rapid transitions between discrete levels (blue signal) at each edge of a clock (dotted line) running at the sampling frequency f_s. The dominant frequency content of this analog waveform is in the 1st Nyquist zone, but significant frequency content exists at image frequencies. If the DAC is capable of flipping the signal to its complement at each falling edge of the clock, moving frequency content moves to higher Nyquist zones and efficiently boosting output power in the 2nd Nyquist zone.*

high frequency signals with a low-pass anti-aliasing filter having a sharp roll-off above f_N. If instead a band-pass filter is used to select one Nyquist zone of interest, we can map the high frequency signal to its alias in the 1st Nyquist zone. With Digital Down-Conversion (DDC) the filter and sampling frequency should be carefully chosen, so as to be absolutely sure of the zone from which the signal actually originates.

Digital Up-Conversion (DUC) is achieved by boosting output power in a higher Nyquist zone. DACs switch between discrete levels at the rising edge of a square-wave clock (see fig. 2). This mode of operation is called non-return to zero (NRZ), or "normal mode". The rapid step generates frequency content at image frequencies: the original signal frequency is mirrored around each multiple of the sampling-clock frequency. Typically the higher frequencies are removed by a reconstruction filter with a rapid roll-off above the Nyquist frequency f_N.

If instead the DAC is constructed to flip the signal about its mid-point at each falling edge of the clock, it will boost the power in the 2nd and 3rd Nyquist zones, while reducing the power in the 1st and 4th zones. This mode of operation is called return to complement (RTC), or "mixed mode". A band-pass reconstruction filter is then used to select the 2nd zone. Here again, the sampling frequency and filter should be carefully chosen to avoid spurious tones outside the zone of interest. Such spurious tones can be quite strong when the tone and its image are close to a zone boundary.

Direct Digital Synthesis (DDS)

Thus, digital circuits can directly reach microwave bands with data converters capable of 10 GS/s. But

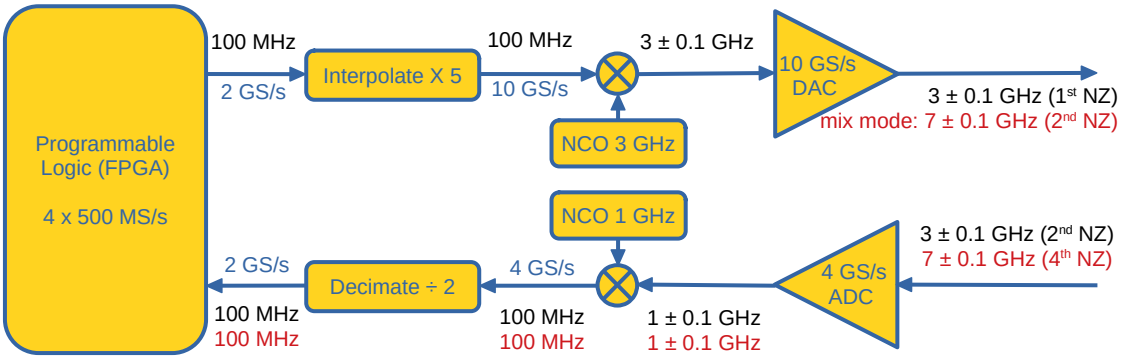


Figure 3: Flow chart showing the conversion steps for digital generation (upper path) and measurement (lower path) of high frequency signals. We follow a 100 MHz signal synthesized by programmable logic at each stage in the conversion path.

state-of-the-art FPGA logic runs at only 500 MHz. Parallel processing of samples bridges this gap between the slow logic and the high-speed converters. Additional flexibility is provided by digital multiplication with a Numerically Controlled Oscillator (NCO). Digital mixing is mathematically perfect so it introduces no distortion or leakage, in stark contrast to analog mixing.

Figure 3 shows a scheme to synchronously generate and measure arbitrary waveforms in a 2 GHz band around a user-selected center frequency. The waveform is first synthesized in the FPGA using 4 parallel data paths, resulting in an effective data rate of 2 GS/s. As an example we consider a 100 MHz signal, but any waveform with frequency content below 1 GHz is possible. The waveform is interpolated by a factor of 5 to an effective date rate of 10 GS/s. We then digitally multiply the signal with a 3 GHz NCO. Any frequency below 5 GHz can be selected for the NCO, with 20 µHz precision. The multiplication results in two side-bands at 3 ± 0.1 GHz, but either side-band can be chosen if both I and Q quadratures of the original waveform are synthesized. Digital mixing results in perfect suppression of unwanted sideband. Thus we can position our signal anywhere in a 2 GHz band centered at the NCO frequency.

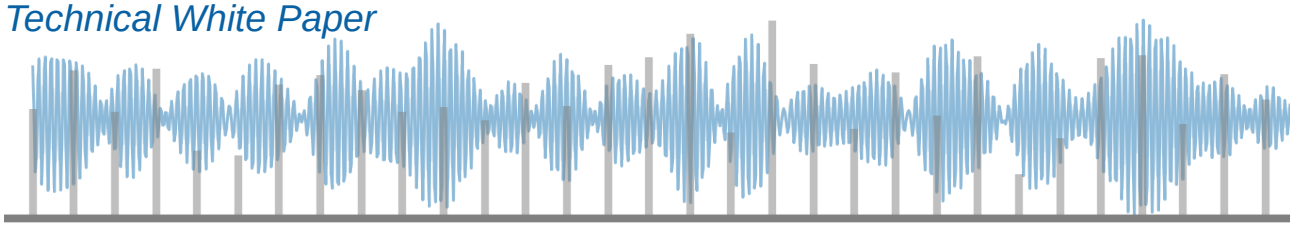
In the final output stage the samples are sent to a 10 GS/s DAC which outputs the high-frequency analog waveform. The sharp steps give frequency content at $f = 3 \pm 0.1$ GHz with an image in the 2nd Nyquist zone at $f_s - f = 7 \pm 0.1$ GHz. The mixed mode of the DAC boosts power in the 2nd NZ while reducing power in the 1st NZ (see fig. 2). An external analog reconstruction filter removes the unwanted band.

The down-conversion of a high-frequency analog signal occurs in a similar manner, but with a slower ADC at 4 GS/s. At this sampling frequency, signals at 3 ± 0.1 GHz or 7 ± 0.1 GHz, in the 2nd and 4th NZ respectively, alias down to the same frequency, 1 ± 0.1 GHz. These two signals are therefore indistinguishable to the ADC.

Our example demonstrates an important precaution with direct digital methods: *one should use an external analog filter to remove signals outside the Nyquist Zone of interest*. At first, this might feel like an added burden. In reality, these filters are usually embedded into traditional designs and thus inaccessible to the end user. With DDS-capable converters, the power and flexibility of choosing the analog filters is given to the end user.

Down-conversion proceeds with multiplication by an NCO at 1 GHz, resulting in a 100 MHz signal which is highly over-sampled at 4 GS/s. With decimation by a factor of 2 we arrive at 2 GS/s, to be analyzed by the FPGA running at 500 MHz with 4 parallel data paths.

Figure 4: The front and back panel showing Vivace's connections: 8 input and 8 output signal ports (14 bit resolution), 4 input and for 4 output ports for digital triggers or markers, clock reference for synchronization to external instruments, and ethernet connection for data transfer. A specification sheet is found here.



Vivace and Presto

Intermodulation Products has developed two new measurement platforms for readout and control of quantum experiments. Based on the latest RFSoC chips from Xilinx, ***Vivace*** (fast and lively) and ***Presto*** (very, very fast) are named with terms notating tempo in music, an art form with many analogs in quantum technology.

Intermodulation Products firmware gives exceptional digital signal processing power through an Application Programming Interface (API) in Python. Numerous features are available at run-time via Python scripting, eliminating the complex and time-consuming task of developing and re-compiling FPGA code.

A pulse-sequencing firmware is designed for phase-coherent pulse generation and readout on multiple ports. Signal generation works with templates that are pre-stored in memory. By looping, concatenating and stretching, waveforms are modified in real-time. *Vivace* or *Presto* can perform rapid parameter searches, calibrations, or execute algorithms by stepping through waveforms and pulse shapes. There is no need to generate giga samples of data on a lab computer and wait for transfer to on-chip memory.

Signal analysis on-chip performs real-time summation (averaging), or multiplication with a template and summation (template matching) for quantum state discrimination. Sinusodial templates give averaged quadrate data. One can simultaneously match with multiple templates and the results of template matches are compared with threshold values. Boolean logic is then used to arm or trigger subsequent events in the measurement sequence, thus enabling low-latency feedback and feed-forward for quantum error correction. With template matching *Vivace* and *Presto* achieve near converter-limited latency of 200 ns.

Signal generation and analysis on all channels is coordinated by a master sequencer with up to 16382 events placed on a temporal axis with 2 ns resolution. 500 ps time resolution is achieved by adjusting samples in a template.

Vivace and *Presto* also come with a continuous-wave firmware, designed for modulating and demodulating at multiple frequencies simultaneously. 192 frequencies can be distributed to the output ports (8 or 16, depending on the chip used). A key innovation is the ability to tune all 192 frequencies, forcing them to be integer multiples of the resolution bandwidth. This feature completely eliminates Fourier leakage between tones separated by only one bandwidth. It also enables lock-in detection at mixing frequencies, to reveal quantum correlations in the frequency domain [2]. The continuous-wave firmware is ideal for many different kinds of frequency-domain measurement, with built-in methods for multifrequency sweeping, for example to rapidly find very high-Q resonances.

Glossary of Acronyms

ADC – Analog to Digital Converter
API – Application Programming Interface
DAC – Digital to Analog Converter
DDC – Digital Down-Conversion
DDS – Direct Digital Synthesis
DSP – Digital Signal Processing
FPGA – Field Programmable Gate Array
GS/s – Giga Samples per second
I and Q – In-phase and Quadrature
LO – Local Oscillator
NCO – Numerically Controlled Oscillator
NZ – Nyquist Zone
RFSoC – Radio Frequency System on a Chip

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[1] Calibration of mixer amplitude and phase imbalance in superconducting circuits. S.W. Jolin, R. Borgani, M.O. Tholén, D. Forchheimer and D.B. Haviland. Rev. Sci. Instrum. **91**, 124707 (2020).

[2] Squeezing and correlations of multiple modes in a parametric acoustic cavity. G. Andersson. S.W. Jolin, M. Scigliuzzo, R. Borgani, M.O.Tholén, D.B. Haviland and P. Delsing. ArXiv:2007.05826v1